<u>Claims</u>

What is claimed is:

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- 1. A semiconductor device, comprising:
 - a substrate of a first conductivity type;
 - a first insulating layer formed on at least a portion of the substrate;

an epitaxial layer of a second conductivity type formed on at least a portion of the first insulating layer;

first and second source/drain regions of the second conductivity type formed in the epitaxial layer proximate an upper surface of the epitaxial layer, the first and second source/drain regions being spaced laterally from one another;

a gate formed above the epitaxial layer proximate the upper surface of the epitaxial layer and at least partially between the first and second source/drain regions;

a first source/drain contact formed through the epitaxial layer and first insulating layer, the first source/drain contact configured so as to be in direct electrical connection with the substrate, the first source/drain region and the epitaxial layer; and

a second source/drain contact formed at least partially through the epitaxial layer, the second source/drain contact configured so as to be in direct electrical connection with the second source/drain region.

- 2. The device of claim 1, wherein the first source/drain contact is configured so as to prevent triggering of a parasitic bipolar transistor associated with the device, the parasitic bipolar transistor including a base-emitter region formed between the substrate and the first source/drain region, and a base-collector region formed between the substrate and the epitaxial layer.
- 3. The device of claim 2, wherein the first source/drain contact prevents triggering of the parasitic bipolar transistor by substantially shorting the epitaxial layer, the substrate and the first source/drain region together.

- 4. The device of claim 1, further comprising a shielding structure formed proximate the upper surface of the epitaxial layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.
- 5. The device of claim 4, wherein the shielding structure is formed substantially concurrently with the gate.

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- 6. The device of claim 4, further comprising a second insulating formed under at least a portion of the gate and the shielding structure.
- 7. The device of claim 6, wherein the second insulating layer formed under the gate and the shielding structure are of different thicknesses relative to one another.
 - 8. The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device.
 - 9. The device of claim 1, wherein the device comprises a laterally diffused MOS (LDMOS) device.
- 15 10. The device of claim 1, wherein the first source/drain region comprises a source of the device and the second source/drain region comprises a drain of the device.
 - 11. The device of claim 1, wherein the epitaxial layer is doped with an impurity having a concentration in a range of about 2×10^{16} to about 2×10^{17} atoms per cubic centimeter.
- The device of claim 1, wherein the first conductivity type is p-type and the second conductivity type is n-type.

13. The device of claim 1, wherein the substrate, first insulating layer and epitaxial layer are formed by a wafer bonding process, whereby a first semiconductor wafer is provided comprising a substrate of the first conductivity type and a second semiconductor wafer is provided comprising a substrate of the second conductivity type, at least one of the first and second semiconductor wafers further comprising at least a portion of the first insulating layer formed on the respective substrates, the second semiconductor being inverted and joined to the first semiconductor wafer at the first insulating layer.

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14. A method of forming a metal-oxide-semiconductor device in a semiconductor wafer, the method comprising the steps of:

forming a first insulating layer on at least a portion of a semiconductor substrate of a first conductivity type;

forming an epitaxial layer of a second conductivity type on at least a portion of the first insulating layer;

forming a gate on an upper surface of the semiconductor wafer;

forming a body region of the first conductivity type in the epitaxial layer proximate the upper surface of the epitaxial layer, the body region being formed at least partially under the gate;

forming first and second source/drain regions of the second conductivity type in the epitaxial layer, the gate being formed above and at least partially between the first and second source/drain regions;

forming a first source/drain contact through the epitaxial layer and first insulating layer, the first source/drain contact being configured such that the first source/drain contact is in direct electrical connection with the substrate, the first source/drain region and the epitaxial layer; and

forming a second source/drain contact at least partially through the epitaxial layer, the second source/drain contact being configured such that the second source/drain contact is in direct electrical connection with the second source/drain region:

- 15. The method of claim 14, further comprising the step of forming a shielding structure proximate the upper surface of the epitaxial layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.
- 16. The method of claim 15, further comprising the step of forming a second insulating layer under at least a portion of the gate and the shielding structure.
- 17. The method of claim 16, wherein the second insulating layer formed under the gate and the shielding structure are of different thicknesses relative to one another.
- 18. The method of claim 14, wherein the step of forming the first source/drain contact comprises the steps of:

forming a first trench through the epitaxial layer and first source/drain region to at least partially expose the first insulating layer;

removing the first insulating layer proximate a bottom wall of the first trench to at least partially expose the substrate; and

substantially filling the first trench with an electrically conductive material.

- 19. An integrated circuit including at least one semiconductor device, the at least one semiconductor device comprising:
 - a substrate of a first conductivity type;

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- a first insulating layer formed on at least a portion of the substrate;
- an epitaxial layer of a second conductivity type formed on at least a portion of the first insulating layer;

first and second source/drain regions of the second conductivity type formed in the epitaxial layer proximate an upper surface of the epitaxial layer, the first and second source/drain regions being spaced laterally from one another;

a gate formed above the epitaxial layer proximate the upper surface of the epitaxial layer and at least partially between the first and second source/drain regions;

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a first source/drain contact formed through the epitaxial layer and first insulating layer, the first source/drain contact configured so as to be in direct electrical connection with the substrate, the first source/drain region and the epitaxial layer; and

a second source/drain contact formed at least partially through the epitaxial layer, the second source/drain contact configured so as to be in direct electrical connection with the second source/drain region.

- 20. The integrated circuit of claim 19, wherein the first source/drain contact is configured so as to prevent triggering of a parasitic bipolar transistor associated with the device, the parasitic bipolar transistor including a base-emitter region formed between the substrate and the first source/drain region, and a base-collector region formed between the substrate and the epitaxial layer.
- 21. The integrated circuit of claim 19, further comprising a shielding structure formed proximate the upper surface of the epitaxial layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.